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CLOCK RECOVERY USING CLOCK PHASE INTERPOLATOR

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Field

The present invention relates generally to clock recovery in communications systems, and more specifically to fine phase control of a recovered clock.

Background of the Invention

Modern integrated circuits are becoming smaller, more dense, and faster. The increased density and speed of integrated circuits (chips) has resulted in chips with internal operating frequencies far higher than external operating frequencies. For example, the internal clock frequencies of some microprocessors have increased from a few megahertz (MHz) 20 years ago, to over one gigahertz (GHz) today, while external operating frequencies have generally stalled at less than 100 MHz.

The overall performance of some integrated circuits is reduced because of lower external operating frequencies. For example, an integrated circuit that transmits or receives a significant amount of data may have to "stall" internal operations while the external interface "catches up" with the faster internal circuitry.

Reliable high speed data transmission between integrated circuits is hampered in part by phase jitter and clock skew as data signals and clock signals travel between the integrated circuits. Circuits have been developed to "recover" the phase of clock signals as they are received by integrated circuits. Clock recovery aids in the alignment of the phase of the clock signal with a received data signal in order to increase reliability of the received data. See, for example, Stephanos Sidiropoulos and Mark A. Horowitz, "A Semidigital Dual Delay Locked Loop," IEEE Journal of Solid State Circuits, Volume 32, No. 11, November 1997. As the external operating frequencies continue to increase, finer phase control in clock recovery circuits can further increase reliability.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the

present specification, there is a need in the art for a method and apparatus to provide fine phase control in clock recovery circuits.

Brief Description of the Drawings

Figure 1 shows an integrated circuit with a clock recovery circuit;

Figure 2 shows a delay locked loop;

Figure 3 shows waveforms produced by the delay locked loop of Figure 2;

Figure 4 shows a clock phase interpolator;

Figure 5 shows another clock phase interpolator;

Figure 6 shows a variable current source;

Figure 7 shows another clock phase interpolator;

Figure 8 is a graph of simulation results showing phase linearity of the clock phase interpolator of Figure 7;

Figure 9 shows a control logic circuit; and

Figure 10 shows a phase comparator.

Description of Embodiments

In the following detailed description of the embodiments, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. Moreover, it is to be understood that the various embodiments of the invention, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described in one embodiment may be included within other embodiments. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined

only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

The method and apparatus of the present invention provide a mechanism to recover a clock signal with fine phase adjustments. A delay locked loop circuit provides multiple clock phases, and a clock phase interpolator circuit interpolates between the clock phases to provide fine phase adjustment. The clock phase interpolator circuit utilizes differential transistor pairs to mix currents from various clock phases to provide the desired phase.

Figure 1 shows an integrated circuit with a clock recovery circuit. Integrated circuit 100 includes delay locked loop 110, clock phase interpolator 120, phase detector 130, and control logic 140.

Delay locked loop 110 receives an input clock on node 112 and produces multiple clock phases on node 114. Node 114, like many nodes throughout the several figures, is shown schematically as a single line, but in implementation, node 114 can be many physical nodes, lines, or traces. In different embodiments of the present invention, delay locked loop 110 produces a different number of clock phases on node 114. For example, in some embodiments delay locked loop 110 produces four clock phases on node 114, and in other embodiments delay locked loop 110 produces eight clock phases on node 114. A delay locked loop is shown and described in mode detail below with reference to Figure 2.

Delay locked loop 110 is an example circuit that can provide multiple clock phases from which to interpolate. Other circuits that produce multiple phases of the clock can be substituted for delay locked loop 110 without departing from the scope of the present invention. For example, a phase locked loop can be utilized to provide multiple phases of the clock.

Clock phase interpolator 120 receives multiple clock phases on node 114 and produces an output clock signal on node 122. Clock phase interpolator 120 also receives interpolator control signals on node 142 from control logic 140. Clock phase interpolator 120 interpolates between the multiple clock phases received on

node 114 as a function of the state of the interpolator control signals. A clock phase interpolator is shown and described in more detail below with reference to Figure 7.

Interpolator control signals on node 142 are produced by control logic 140 in response to a phase error signal on node 132 produced by phase detector 130. Phase detector 130 produces the phase error signal on node 132 in response to an input data signal on node 134 and the output clock signal on node 122. A control logic circuit and a phase detector are shown and described in more detail below with reference to Figures 9 and 10, respectively.

The circuit shown in Figure 1 can be useful to provide fine phase control of the output clock signal on node 122, thereby allowing a close phase match between the output clock signal on node 122 and the input data on node 134. In some embodiments, the input data on node 134 and the input clock signal on node 112 are received from points external to integrated circuit 100. In these embodiments, the circuit of Figure 1 is a clock recovery circuit that recovers the clock phase that aligns with the input data. For example, the circuit of Figure 1 can be useful to capture a data stream of unknown phase entering integrated circuit 100.

In other embodiments, the input data on node 134 and the input clock on node 112 are received from other circuits within integrated circuit 100. In these embodiments, the circuit shown in Figure 1 is a clock recovery circuit that recovers the phase of data internal to integrated circuit 100. For example, the circuit of Figure 1 can be useful for recovering clocks of varying phases within a data path of a microprocessor.

In some embodiments, multiple input data signals are received, and a single input data signal is used in the clock recovery circuit. For example, input data signal on node 134 can be a least significant bit of a 32 bit data bus, where the other 31 data bits are not utilized for clock recovery. In other embodiments, each input data signal has associated therewith a clock recovery circuit such as represented in Figure 1. In very high speed applications, a separate clock recovery circuit for each input data signal can be useful to produce separate clock signals, each having a phase matched to a separate input data signal.

Integrated circuit 100 can be any type of integrated circuit capable of including a clock recovery circuit. For example, integrated circuit 100 can be a processor such as a microprocessor, a digital signal processor, a microcontroller, or the like. Integrated circuit 100 can also be an integrated circuit other than a processor such as an application-specific integrated circuit (ASIC), a communications device, a memory controller, or a memory such as a dynamic random access memory (DRAM).

Figure 2 shows a delay locked loop (DLL). DLL 200 is an example embodiment of a delay locked loop suitable for use as delay locked loop 110 (Figure 1). DLL 200 includes phase detector 210 that receives an input clock on node 208 and a feedback clock on node 206. In response to a phase difference between the two input clock signals, phase detector 210 produces a DLL control voltage on node 220. The DLL control voltage on node 220 controls a delay of variable delay elements 212, 214, 216, and 218. Variable delay elements 212, 214, 216, and 218 produce different phases of the input clock signal on nodes 222, 224, 226, and 228, respectively.

In embodiments represented by Figure 2, four separate clock phases are generated, labeled P0, P1, P2, and P3. These clock phases correspond to the multiple clock phases on node 114 (Figure 1). Also in the embodiments represented by Figure 2, four variable delay elements are included that provide a delay substantially equal to 180° of phase shift at the frequency of the input clock. This provides four clock phases at substantially 45° increments, shown as 0°, 45°, 90°, and 135° in Figure 3. In other embodiments, more or less than four variable delay elements can be included, thereby providing finer phase control out of DLL circuit 200. Furthermore, in other embodiments, the sum of the delay of the variable delay elements can be equal to 360° of the input clock signal, thereby providing more output phase signals. In general, any number of variable delay elements can be included without departing from the scope of the present invention.

Figure 3 shows waveforms produced by the delay locked loop circuit of Figure 2. Waveform 310 corresponds to the input clock signal on node 208.

Likewise, waveform 320 shows the phase relationship of the clock signal on node 222, waveform 330 shows the phase relationship of the clock signal on node 224, waveform 340 shows the phase relationship of the clock signal on node 226, and waveform 350 shows the phase relationship of the clock signal on node 228. Clock signals are provided at 0°, 45°, 90°, and 135°. In some embodiments, the phase signals output from delay locked loop 110 (Figure 1) are differential signals. This is illustrated in Figure 2 where each clock phase is shown having two nodes. In embodiments that include differential signals, additional phase angles can be achieved by inverting the differential signals. For example, P0 can be inverted to produce a clock phase at 180°, P1 can be inverted to produce a clock signal at 225°, P2 can be inverted to produce a clock signal at 270°, and P3 can be inverted to produce a clock signal at 315°.

Figure 4 shows a clock phase interpolator. Clock phase interpolator circuit 400 includes differential transistor pairs 402, 412, 432, and 442, select transistors 404, 414, 434, and 444, current sources 420 and 450, load devices 460, and differential amplifier 470. Differential transistor pair 402 receives the differential signal P0 on node 222 (Figure 2) as an input signal. Likewise, differential transistor pair 432 receives P1, differential transistor pair 412 receives P2, and differential transistor pair 442 receives P3. Each of the clock phase signals (P0-P3) includes a clock signal and its complement to form a differential pair. For example, Px and Px# form the differential pair for Px, where x is a value from 0 to 3. This naming convention is used throughout this description. Select transistors 404, 414, 434, and 444 are each responsive to a control signal labeled SEL0, SEL2, SEL1, and SEL3, respectively. The SEL signals are control signals provided by control logic such as control logic 140 (Figure 1).

The differential transistor pairs shown in Figure 1 include n-channel isolated gate field effect transistors. In some embodiments, the n-channel isolated gate field effect transistors are n-channel metal oxide semiconductor field effect transistors (NMOSFETs). The choice of NMOSFETs for use in the figures is strictly one of convenience. The method and apparatus of the present invention can be practiced

with other types of components such as p-channel isolated gate field effect transistors and bipolar junction transistors. A great number of suitable component types exist to practice the various embodiments of the invention, and a choice of any of these component types can be made without departing from the scope of the present invention.

Different differential transistor pairs can be selected using the select transistors. As a result, the current sourced by current sources 420 and 450 is switched between the various differential transistor pairs. For example, when select transistors 404 and 434 are on, and select transistors 414 and 444 are off, differential transistor pairs 402 and 432 have current flowing therethrough and differential transistor pairs 412 and 442 do not have current flowing therethrough. Differential transistor pair 402 switches current between nodes 410 and 411 at the frequency of the input clock signal and at the phase of the clock phase signals that drive differential transistor pair 402. Likewise, differential transistor pair 432 switches current between nodes 410 and 411 at a clock phase equal to the phase of the signal driving differential transistor pair 432. In the example just described, one differential transistor pair is switching current at a phase of 0°, and a second differential transistor pair is switching current at 45°. These currents on nodes 410 and 411 produce a voltage across load devices 460. The voltages across load devices 460 are input voltages to a differential amplifier 470. Differential amplifier 470 provides an output clock signal on node 472. The phase of the output clock signal on node 472 is substantially equal to the center point between the two differential transistor pairs selected. For example, when differential transistor pairs 402 and 432 are selected, the output clock signal on node 472 is at substantially 22.5° plus any delay attributable to differential amplifier 470.

Differential transistor pairs 402 and 412 form a first plurality of differential transistor pairs coupled to a current source through select transistors. Each of differential transistor pairs 402 and 412 are connected to the same current source 420 through select transistors 404 and 414. Likewise, differential transistor pairs 432 and 442 form a second plurality of differential transistor pairs coupled to a current source

through select transistors. Each of differential transistor pairs 432 and 442 are connected to current source 450 through select transistors 434 and 444.

Load devices 460 are shown as resistors in Figure 4. In some embodiments, load devices 460 are active load devices such as transistors. In general, load devices 460 can be any circuit or sub-circuit that provide a load to allow a voltage to be developed at the inputs to differential amplifier 470.

In operation, one of the first plurality of differential transistor pairs is selected and one of the second plurality of differential transistor pairs is selected to provide an output clock signal on node 472 with an interpolated phase. The phase of the output clock signal is interpolated between the two differential transistor pairs selected. In the example set forth above, differential transistor pairs operating at 0° and 45° were selected to yield an output clock signal at substantially 22.5°. The control logic driving the select transistors select the differential transistor pairs having the desired phase relationship to produce an output clock signal on node 472 having the desired phase.

In embodiments represented by clock phase interpolator 400, four clock phases are received, and interpolation is provided between each of the four clock phases. In other embodiments, more than four clock phases are provided. In some embodiments, this corresponds to a delay locked loop having more than four variable delay elements. In other embodiments, it corresponds to the utilization of additional clock phases available through the inversion of differential signals. One such utilization is shown and described below with reference to Figure 7.

Figure 5 shows another clock phase interpolator. Clock phase interpolator 500 includes differential transistor pairs 502 and 512, load devices 560, and differential amplifier 570. Differential transistor pairs 502 and 512 each receive a clock signal having a desired phase relationship. In the example shown in Figure 5, differential transistor pair 502 receives P0 at 0° and differential transistor pair 512 receives P1 at 45°.

Current provided by current source 520 is switched between the transistors in differential transistor pair 502 and current provided by current source 550 is switched

between the transistors and differential transistor pair 512. These currents combine on nodes 510 and 511 to produce voltages across load devices 560. These voltages are input to differential amplifier 570 which produces an output clock signal on node 572. Current sources 520 and 550 are variable current sources, each having a current set by signals on current source control nodes 522 and 552. The current source control data on nodes 522 and 552 is provided by a control logic circuit such as control logic circuit 140 (Figure 1).

By varying the amount of current sourced by current sources 520 and 550, the clock phases input to differential transistor pairs 502 and 512 can be mixed by varying amounts to produce a variable phase on the output clock signal on node 572. For example, when current source 520 provides more current than current source 550, the output clock signal will have a phase closer to that of P0 than to P1. Likewise, when current source 550 sources more current than current source 520, the output clock signal will have a phase closer to that of P1 than to P0.

In the embodiments represented by Figure 5, two differential transistor pairs exist, each receiving a clock signal at a different phase. As shown in Figure 5, the two clock phases are represented as 0° and 45°. Any clock phase can be used without departing from the scope of the present invention. For example, differential transistor pair 502 can receive a clock phase at 135°, and differential transistor pair 512 can receive a clock signal at 145°, thereby allowing an output clock signal to be interpolated between these two phases.

Figure 6 shows a variable current source. Current source 600 includes a plurality of selectable current source circuits. For example, one selectable current source circuit includes current source transistor 602 and select transistors 604 and 606. Likewise, another selectable current source circuit includes current source transistor 612 and select transistors 614 and 616. Furthermore, another selectable current source circuit includes current source transistor 622 and select transistors 624 and 626. Current source 600 is shown having three selectable current source circuits, but any number of selectable current source circuits can be included without departing from the scope of the present invention. Variable current source 600 can

be utilized as a variable current source such as current source 520 or 550 (Figure 5). In these embodiments, the signals shown controlling pass transistors 604, 606, 614, 616, 624, and 626 are current source control signals provided to vary the amount of current 632 supplied by variable current source 600 on node 630.

In operation, a current source transistor is selected by varying the signals controlling the select transistors connected thereto. For example, current source transistor 602 has a gate coupled to a bias voltage through select transistor 604 and coupled to a reference potential through select transistor 606. When control signal A1 is asserted, select transistor 604 conducts and select transistor 606 does not. As a result, current source transistor 602 has the bias voltage imposed from gate to source thereby providing a current that contributes to current 632 on node 630. When control signal A1 is de-asserted, select transistor 604 is off and select transistor 606 is on, thereby coupling the gate of current source transistor 602 to the reference potential and turning current source transistor 602 off.

Any number of current source transistors can be on, and any number of current source transistors can be off, based on the values of the control signals shown in Figure 6. In embodiments represented by Figure 6, each current source transistor sources substantially the same current when the bias voltage is applied to the gate. In other embodiments, different bias voltages are provided to the different current source transistors, thereby providing a different weight to each selectable current source circuit. In still other embodiments, each current source transistor is a different size, thereby providing a different amount of current from the same bias voltage. For example, each current source transistor can be sized in a binary fashion such that a binary control word can be applied to variable current source 600 to provide a greater range of current values.

Figure 7 shows another clock phase interpolator. Clock phase interpolator 700 includes two pluralities of differential transistor pairs, each coupled to a variable current source through select transistors. For example, differential transistor pairs 702, 706, 710, and 714 are each coupled to variable current source 720 through select transistors 704, 708, 712, and 716, respectively. Likewise, differential transistor

pairs 722, 726, 730, and 734 are coupled to variable current source 750 through select transistors 724, 728, 732, and 736, respectively. As shown in Figure 7, the plurality of differential transistor pairs coupled to variable current source 720 correspond to clock phases of 0°, 90°, 180°, and 270°. Clock phases of 0° and 90° are provided by clock phase signals in the same manner as previously described with reference to Figure 4. Clock phase signals of 180° and 270° are provided by logically inverting the clock phase signals that provide 0° and 90°, respectively. The logical inversion is accomplished by switching the ordering of connections of the differential signals. For example, differential transistor pair 702 has P0 connected to the leftmost transistor and P0# connected to the rightmost transistor, whereas the connections are reversed for differential transistor pair 710. The second plurality of differential transistor pairs provides clock phases of 45°, 135°, 225°, and 315° in the same manner.

In operation, one of the first plurality of differential transistor pairs is selected using one of select transistors 704, 708, 712, and 716, and one of the second plurality of differential transistor pairs is selected using select transistors 724, 728, 732, and 736. These two clock phases are mixed by varying amounts based on the currents sourced by variable current sources 720 and 750. For example, an output clock with a relative phase of between 90° and 135° can be achieved by selecting differential transistor pairs 706 and 726 using select transistors 708 and 728, respectively, and varying the current provided by variable current sources 720 and 750 using current source control signals on nodes 722 and 752, respectively. The currents switched by the two differential transistor pairs are summed at nodes 710 and 711, thereby producing voltages across load devices 760. These voltages are sensed by differential amplifier 770 to produce an output clock signal on node 772 with the desired phase.

The control signals for clock phase interpolator 700 include select signals to turn on and off select transistors, and current source control signals on nodes 722 and 752. These control signals are digital signals that can be provided by any suitable digital circuit. For example, in some embodiments, the control signals shown in

Figure 7 correspond to the interpolator control signals on node 142 (Figure 1). Control signals having digital voltage levels can be useful for many reasons, including the ability to test the output clock phase under controlled laboratory conditions using readily available digital test equipment.

Clock phase interpolator 700 accomplishes the interpolation of clock phases in one circuit stage, reducing both power consumption and jitter. By selecting two differential transistor pairs, static power is reduced to that consumed by two transistor pairs, and by performing the interpolation in a single circuit, jitter commonly caused by power supply noise in digital components is reduced.

Figure 8 is a graph of simulation results showing phase linearity of the clock phase interpolator of Figure 7. Graph 800 shows the output clock phase angle 810 at 56 different interpolator control signal settings. The interpolator control signal settings correspond to the select signals and the current source control signals shown in Figure 7. In some embodiments, these interpolator control signals correspond to the interpolator control signals on node 142 as shown in Figure 1.

The 56 different settings for the interpolator control signals allow an average resolution of 6.4° across a 360° range. In other embodiments, higher resolution can be obtained through either increasing the resolution of the variable current sources, or increasing the number of available clock phases and corresponding differential transistor pairs.

Figure 9 shows a control logic circuit. Control logic circuit 900 corresponds to a control logic circuit for use in a clock recovery circuit such as control logic 140 (Figure 1). Control logic circuit 900 includes analog to digital converter (A/D) 910, state machine 920, scan data register 930, and multiplexor 940. In embodiments represented by control logic circuit 900, the phase error signal on node 902 received from the phase detector is an analog voltage. A/D 910 receives the analog phase error signal on node 902 and provides a digital signal on node 912 to state machine 920. In response thereto, state machine 920 produces interpolator control signals on node 922. Multiplexer 940 selects between interpolator control signals on node 922 and scan data on node 932. In normal operation, multiplexer 940 selects interpolator

control signals on node 922 that are produced by state machine 920. When undergoing test, multiplexer 940 receives signals on node 932 from scan data register 930.

State machine 920 can include any logic, sequential or otherwise, suitable to produce interpolator control signals from the data on node 912. Examples include finite impulse response (FIR) filters, decoders, multiplexers, or sequential state machines. In some embodiments, control logic circuit 900 receives digital data on node 902 from the phase detector. In these embodiments, control logic circuit 900 does not include an analog to digital converter, and state machine 920 receives digital data from the phase comparator directly.

Control logic circuit 900 is useful to provide interpolator control signals to a clock phase interpolator from either closed loop operation, or from test data. Although scan data register 930 is shown separate from state machine 920, in some embodiments, the scan registers are included as part of state machine 920. In these embodiments, interpolator control signals are produced directly from state machine 920 and multiplexor 940 is omitted.

Figure 10 shows a phase comparator suitable for use as phase detector 130 (Figure 1). Comparator 1000 includes a first amplifier stage 1102 and a second amplifier stage 1104. In some embodiments, first amplifier stage 1102 includes differential amplifier 1106, switch 1114, and non-linear load 1116. Differential amplifier 1106 includes a pair of input nodes 1108 and 1109 and a pair of output nodes 1111 and 1112. Switch 1114 and non-linear load 1116 are connected across the pair of output nodes 1111 and 1112.

Differential amplifier 1106 is not limited to a particular type of differential amplifier. In some embodiments, differential amplifier 1106 includes a high-gain linear differential amplifier. For example, in some embodiments, differential amplifier 1106 includes a differential pair of transistors, such as isolated gate field effect transistors. In other embodiments, differential amplifier 1106 includes multiple differential pairs of transistors configured in parallel. In some embodiments, these multiple pairs are n-channel isolated gate field-effect transistors.

In still other embodiments, differential amplifier 1106 includes bipolar junction transistors. Utilizing a differential pair of transistors or multiple differential pairs in parallel allows first amplifier stage 1102 to have a high bandwidth.

In operation, differential amplifier 1106 receives a DATA IN signal and a DATA IN # signal at the pair of input nodes 1108 and 1109, respectively, and generates an amplified signal at the pair of output nodes 1111 and 1112 by amplifying the difference between the DATA IN signal and the DATA IN #. DATA IN and DATA IN # are complementary signals that together form a differential signal that corresponds to DATA IN on node 124 (Figure 1). Differential amplifier 1106 also receives a CLOCK IN signal on node 1113. This CLOCK IN signal corresponds to the clock signal on node 122 (Figure 1).

Switch 1114 receives the clock signal on node 113, and is coupled to nodes 1111 and 1112. Switch 1114 is not limited to a particular type of switch. In some embodiments, switch 1114 is an electronically controllable switch. For example, switch 1114 can be implemented with an isolated gate field-effect transistor having a gate node coupled to node 1113, and source and drain nodes coupled between nodes 1111 and 1112. In other embodiments, switch 1114 is an optically controllable switch. For example, switch 1114 can be implemented with a photo-transistor. Using an optically controllable switch such as a photo-transistor for switch 1114 in comparator 1000 reduces the electrical noise in comparator 1000 by eliminating an electrical signal transmission line and the noise associated with an electrical signal transmission line from comparator 1000.

In operation, switch 1114, when closed, provides a conductive path between nodes 1111 and 1112 to equalize the potential at nodes 1111 and 1112. Switch 1114 can be closed by applying an electronic clock signal (not shown) to the gate of an isolated gate field-effect transistor switch, or by applying an optical clock signal (not shown) to the base (not shown) of a photo-transistor switch.

Non-linear load 1116 is not limited to a particular type of non-linear load. In some embodiments, non-linear load 1116 includes a pair of cross-coupled *n*-channel, isolated gate field-effect transistors. In other embodiments, non-linear load 1116

includes a pair of cross-coupled bipolar junction transistors. In operation, non-linear load 1116 allows the signals at output nodes 1111 and 1112 to reach the supply voltages (not shown) and supports a higher slew rate or bandwidth for signals at output nodes 1111 and 1112 than a linear load.

Second amplifier stage 1104 is coupled to the pair of output nodes 1111 and 1112 of first amplifier stage 1102. Second amplifier stage 1104 includes a pair of second stage input nodes 1170 and 1172, a pair of second-stage output nodes 1174 and 1176, a pair of cross-coupled n-channel isolated gate field-effect transistors 1178 and 1180, a pair of cross-coupled p-channel isolated gate field-effect transistors 1182 and 1184, a switch 1186, and an input pair of n-channel isolated gate field-effect input transistors 1188 and 1190. The input pair of n-channel isolated gate field-effect input transistors 1188 and 1190 are coupled to the input nodes 1170 and 1172. The n-channel isolated gate field effect input transistor 1188 is connected in parallel with the n-channel isolated gate field-effect transistor 1178, and the n-channel isolated gate field-effect input transistor 1190 is connected in parallel with the n-channel isolated gate field-effect transistor 1180. The pair of cross-coupled p-channel isolated gate field-effect transistors 1182 and 1184 and the switch 1186 are connected between the second stage output nodes 1174 and 1176. Second amplifier stage 104 produces output signals DATA OUT and DATA OUT #, which form a differential signal that corresponds to the phase error signal on node 132 (Figure 1).

Switch 1186 is coupled between nodes 1174 and 1176, and receives a delayed clock signal. In some embodiments, the delayed clock signal is a delayed version of CLOCK IN on node 1113. For example, the delayed clock signal can be generated using two inverters (not shown) coupled in series between node 1113 and the delayed clock signal input on switch 1186.

Second amplifier stage 1104 is a non-linear amplifier. Combining a non-linear load in a first amplifier stage with a non-linear amplifier in the second stage amplifier allows the comparator to have a high gain.

In operation, phase comparator 1000 alternates between equalization phases and evaluation phases. For example, when the CLOCK IN signal is asserted, switch

1114 closes and equalizes the potential between nodes 1111 and 1112. Shortly thereafter, switch 1186 closes and equalizes the potential between nodes 1174 and 1176. The equalization phase occurs when switches 1114 and 1186 are closed. When the CLOCK IN signal is de-asserted, switch 1114 opens and nodes 1111 and 1112 begin to change state in response to the state of the input signals on nodes 1108 and 1109. Shortly thereafter, switch 1186 opens and second amplifier stage 1102 amplifies the difference between the signals on nodes 1170 and 1172. The evaluation phase occurs when both switches 1114 and 1186 are open.

It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reading and understanding the above description. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.